National Institute of Technology, Durgapur

Workshop on CMOS Design Using HiSIM MOS Model

CMOS Integrated Circuit business in a fabless design environment is rapidly increasing internationally. In this activity SPICE has emerged as the standard Circuit Simulator where for the simulation of the CMOS circuits MOSFET model provides the interface and communication link between the circuit design community and the prototyping fab. It is obvious that the MOSFET model must represent the device behavior as truly as possible for the CMOS System on Chip (SoC) to work to its specifications.

Fabless design option provides unique opportunity to university communities to realize complex CMOS SoCs printed on silicon chips using industry standard manufacturing facilities.

There are varieties of MOSFET models available to CMOS designers- the model consumers- that necessitates education on the models. The models currently in circulation are BSIM family, HiSIM, EKV etc. MOSFET devices have structures such as bulk, thin film (SOI), high voltage which depends on the areas of applications. Each structure requires corresponding model. Compact Model Coalition (CMC) is a platform which undertakes the standardization activity.

The present workshop is focused on discussion and understanding of HiSIM model pioneered by Hiroshima University. Prof. Meiura Mitiko Mattausch who proposed the model, will be presenting the features of HiSIM model for all three variations of MOSFET structures i.e. Bulk, thin film(SOI) and high voltage(HV). HiSIM happens to be the approved standard for high voltage CMOS by CMC. HiSIM presentation will also be preceded by a short overview of MOSFET models by Prof. A.B. Bhattacharyya, Chairman BoG, NIT Durgapur. The workshop is also expecting participation of CAD tool vendors such as Silvaco, Synopsis, Mentor Graphics etc. to participate for discussion on supporting models in their tools. A short simulation session with HiSIM model is being contemplated.

VLSI design community having interest in RF CMOS design, high performance logic, high voltage power electronic chip etc. will find the workshop relevant and useful. The workshop is being organized by the "VLSI design interest group" belonging to ECE, EE, CSE, IT and Physics departments and coordinated by Prof. Ashis Kumar Mal (a.k.mal@IEEE.org) at NIT Durgapur.

National Institute of Technology Durgapur, India

HIROSHIMA UNIVERSITY

CMOS Design Using HiSIM MOS Model

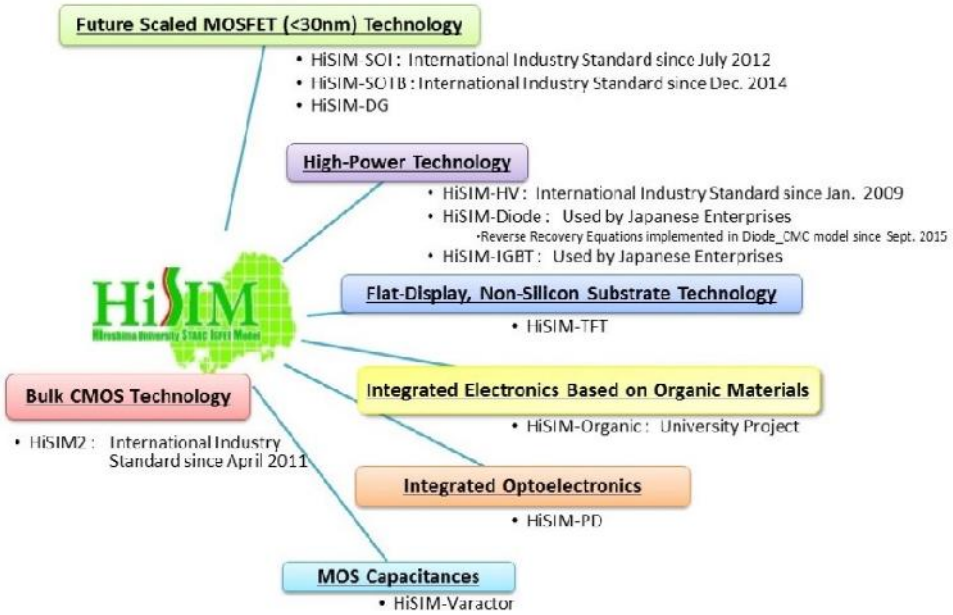
March 10, 2016
National Institute of Technology Durgapur, India

The Department of Electronics & Communication Engineering (ECE) at National Institute of Technology Durgapur, in collaboration with Hiroshima University, is pleased to announce a Workshop on Ideas on Simulation for Designing and Compact Modeling with HiSIM, to be held on March 10, 2016 in NIT Durgapur. Mr. Y. Iino and Prof. Mitiko Miura-Mattausch are among the notable speakers in the workshop.

The focus of this workshop is to introduce students and researchers to the Compact Modeling with **HiSIM Model targeted to Chip design with emphasis on RF and High Voltage designs**. This workshop will be organized around the following sessions:

- Simulation from Device to Circuit
- Compact Modeling : Bulk CMOS, Thin-Film Transistor (SOI) and High Voltage MOSFETs
- Support Circumstances : Design Tools – Mentor Graphics and Foundry Support – AMS
- Application Examples using Spectre/HSPICE/ELDO

Each session will consist will of 1.5-2 Hrs duration.



Please mark your calendar for this event and contact Prof. Ashis K. Mal, Prof. Rajat Mahapatra (a.k.mal@IEEE.org: 94-347-880126), if you are interested in participation. To register online, please use the form (to be updated). For more information visit: http://ece.nitdgp.ac.in

Support for the workshop is provided by TEQIP-II.

TEQIP-Phase II,
NIT Durgapur

HiSIM Hiroshima University STARC IGFET Model

National Institute of Technology
Durgapur, India

HIROSHIMA UNIVERSITY

Distinguished Speakers

Yoshihisa Iino is a Staff Engineer at Silvaco Japan and has been employed at the company for 20 years. Yoshihisa Iino received his B.S. degree in electrical engineering under the guidance of Prof. Katsufusa Shono's from Sophia University, Tokyo, Japan. Since he joined Silvaco, he has been in charge of the Utmost device characterization and SPICE modeling product. Prior to joining Silvaco Japan, he worked at a bipolar IC company and was tasked with establishing a CMOS technology development platform which included the use of Silvaco tools. Prior to this he worked at Texas Instruments Japan Limited, where he was a principal characterization engineer for the extended drain MOS device technology and was responsible for defining process conditions and layout design rules.

Mitiko Miura-Mattausch (M'96–SM'00–F'07) received the Dr.Sc. degree from Hiroshima University, Hiroshima, Japan. Between 1981 to 1984, she was a Researcher with the Max Planck Institute for solid-state physics in Stuttgart, Germany, where she was working with nonlinear phenomena in solid state materials. From 1984 to 1996, she was with the Corporate Research and Development, Siemens AG, Munich, Germany, where she worked on the hot-electron problems in MOSFETs, the development of bipolar transistors, and the analytical modeling of deep submicron MOSFETs for circuit simulation. Since 1996, she has been a Professor with the Department of Semiconductor Electronics and Integration Science, Graduate School of Advanced Sciences of Matter, Hiroshima University, Japan, where she is currently leading the ultra-scaled-device laboratory. She is the author of more than 300 papers in peer-reviewed international journals and conferences, and three technical books. Her major contribution to the society is the development of compact models HiSIM. Four HiSIM models have been already standardized by the Compact Model Coalition (CMC) and are intensively utilized by the international semiconductor and electronics industry since 2008. She was honored for her scientific achievements by several awards such as the purple ribbon award of the Japanese government. She is an IEEE fellow since 2007, and served as an IEEE distinguished lecturer for more than ten years..